The GARDA Project

Building a Galileo Receiver

GARDA consortium at the Final Presentation

The long history of the Galileo program's development has tended to focus on the design, construction, and launch of the system's satellites. But an equally important activity is the development of Galileo-capable user equipment. Leaders of an engineering team that has developed a multi-frequency Galileo receiver describe their efforts and the results.

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As Galileo satellites begin reaching orbit and transmitting their signals, a critical complement needs to be in place for the user community: Galileo-capable receivers. In the frame of Europe's development, of Galileo, the Galileo Joint Undertaking (GJU) has issued three calls since 2003 under the European Commission's 6th Framework Program to study, design, and develop the essential technologies, components, applications, and services for the Galileo user segment.

In response to the first call, Alcatel Alenia Space Italia (AASI) was selected to lead a consortium responsible for developing Galileo receiver technologies within the (GAlileo user Receiver Development Activities (GARDA) program. Table 1 lists consortium members and their responsibilities in GARDA.

Within the GARDA project, AASI has developed a prototype receiver capable of processing L1, E5a/E5b, and E6 Galileo signals in addition to GPS L1. This represents one of the first GPS/Galileo receivers. In developing this prototype receiver, efforts have been made to define the architecture of the RF front-end and baseband sections to be as flexible as possible.

The aim of the GARDA project was to develop a modular architecture that could be the basis for future AASI GPS/Galileo receiver products and prepare the way for user receivers to be "ready on the market" when the Galileo system becomes operational. The design flexibility also allows a quick reaction to the evolution and changes in the Galileo signal specification.

In particular, the GARDA design is the basis for the on-going development of a safety-of-life (SoL) receiver within the GJU's Galileo Integrity Receiver for Advanced Safety Of Life Equipment (GIRASOLE) project. Further, GARDA receivers are going to be used within the Galileo receiver chain of the ground mission segment sensor stations to feed data to the Galileo orbit determination, integrity and timing facilities.

The GARDA project has also provided the opportunity to analyze future market of Galileo applications, to study some core receiver processing techniques and also to develop two important components such as the Galileo RF signal simulator as well as a complete

Galileo receiver and environment SW simulation tool.

This article will describe the design and testing of the receiver technology developed under the GARDA program. We will begin by describing the design challenges and core technologies identified as crucial for receiver development. Then we will address the receiver architecture, functions, and designs developed and tested in a prototype system before implementation in the final product. A section of the article addresses the development of two GNSS simulators as part of the GARDA initiative. These simulators were used to help in testbench design and development of the receivers as well as in testing and performance verification, along with commercial simulators. The article will conclude with a discussion of key results from test evaluations of the GARDA receiver.

Core Technologies

Due to the new Galileo signal-in-space (SIS) structure, Galileo receivers will have to operate and process navigation signals that differ substantially from GPS C/A code by different chipping rates, introduction of pilot signal components or different signal formats, such as binary offset carrier or BOC(1,1) on in the L1 frequency band and Alt-BOC(15,10) on the E5a and E5b bands. Consequently, GARDA identified core technological areas considered essential for future Galileo receivers, including a subset of selected topics with respect to signal processing. Table 2 summarizes these focus technologies together with the corresponding receiver types targeted for application of them..

Code acquisition and code & carrier phase tracking. Code acquisition, as well as code & carrier phase tracking, are fundamental signal processing functions of any navigation receiver. The GARDA studies have focused on various acquisition and tracking strategies that exploit the properties of the new Galileo signal structures, particularly, on L1 and E5.

Our efforts placed special emphasis on the development of algorithms that lead not only to good performance figures but also to a required hardware structure providing maximum commonality with corresponding GPS processing.

Multipath mitigation. In particular, professional and safety-of-life applications with requirements for high accuracy will benefit from effective multipath mitigation techniques. In GARDA, the performance of various multipath mitigation strategies on signal processing level has been extensively studied, with specific focus on techniques that adequately support multipath mitigation for the BOC(1,1) signal on Galileo L1. As a result, these efforts determined that a combination of a "narrow correlator" discriminator with a multipath estimation unit leads to promising performance.

Cross-Correlation Mitigation. Depending on the application, future GNSS navigation receiver performance may be affected by quite different interference sources. While for aeronautical applications the terrestrial radio navigation system DME/TACAN and a military communication system JTIDS may represent major interference sources, navigation receivers using signals on E6 may be mainly affected by pulsed interference from L-band radar.

For terrestrial mobile applications using consumer/mass market receivers that operate in environments characterized by severe shadowing, navigation performance — in particular, the receiver's acquisition capability — will most likely suffer from intra-system interference. This will arise from cross-correlation interference due to substantially different received GNSS signal power levels.

GARDA studies on cross-correlation mitigation have consequently been focused on consumer/mass market receivers employing Galileo L1 signals only. As those receivers commonly use 1-bit analog/digital convertors (ADCs), a multipath mitigation approach has been proposed that can still operate assuming 1-bit input quantization. As could be shown for a quite severe interference scenario, by using the proposed mitigation technique, the effect of cross-correlation on the acquisition performance may be reduced to an almost negligible level.

Company/Institute	Activity
Alcatel Alenia Space Italia	Receiver & Core Technologies
Deimos Space	GRANADA SW Simulator
Audens Act	Core Technologies
Space Engineering	Galileo RF Signal Simulator
Satimo	Antenna
Booz Hallen Hamilton	Market Analysis & Rx Development Plan
Politecnico di Torino	Core Technologies
Prague Technical Univ.	Core Technologies
ST Microelectronics	Consumer applications
Advanced Aviation Tech.	Certification and Safety

TABLE 1. GARDA consortium partners and tasks

Core Technology	Receiver Types
Code & Carrier Phase Tracking	all
Code Acquisition	all
Multipath Mitigation	professional, safety-of-life
Cross-Correlation Mitigation	consumer/massmarket
Positioning with limited signal	consumer/massmarket
Hybrid PVT	consumer/massmarket
Measurements Quality Control	professional, safety-of-life

TABLE 2. Core Technological Topics studied by GARDA

Advanced positioning with limited signals and hybrid PVT. User equipment targeting the consumer mass market will mainly take the form of small, low-cost navigation-only receivers using single-frequency Galileo and/or GPS L1 signals, or will be integrated into handheld communication user terminals. Particularly for combined navigation/communications (NAV/COM) mobile terminals, positioning may be only required if, for example, a location-based service (LBS) is initiated. In this case "one-shot" positioning is apparently preferable, because of the savings in power consumption.

In GARDA, researchers extensively studied the performance of various approaches to advanced positioning with

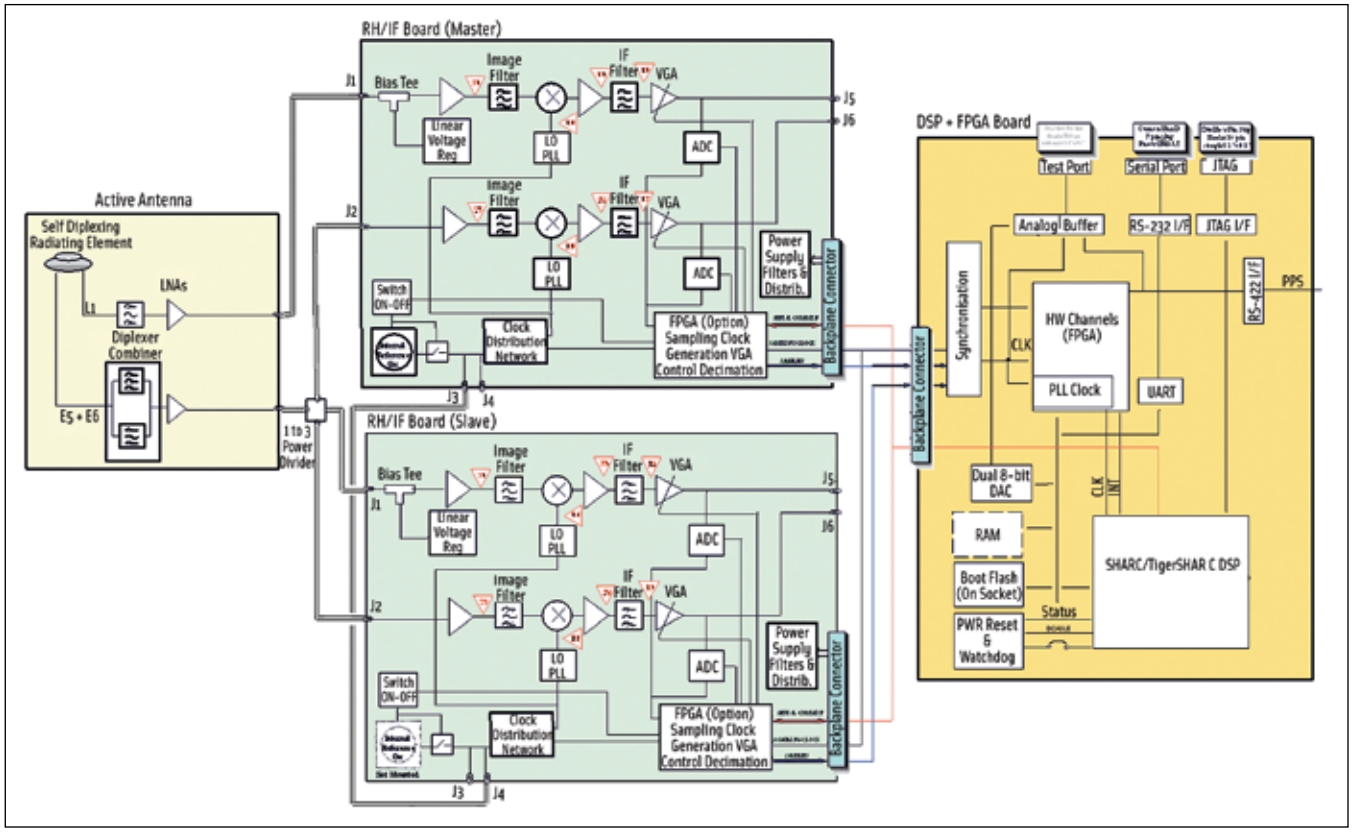


FIGURE 1 Receiver Block Diagram

limited signals, with a focus on adapting promising techniques to the new Galileo L1 signal structure. Combined NAV/COM mobile terminals may achieve a higher integration of navigation and terrestrial communications by basing positioning/velocity/timing (PVT) solutions not only on GNSS signals-in-space but also on data derived from the communication network — so-called assisted GNSS. By exploiting both, the availability of correct navigation information may be considerably improved, especially for environments in which the reception of a sufficient number of satellite signals can not always be ensured. This was the subject of detailed study in GARDA.

Measurement Quality Estimation/Control. Measurement quality control is considered an essential feature for professional and safety-of-life receivers, in order to control the accuracy, reliability, and integrity of the determined PVT solutions. Accordingly, in GARDA detailed analyses focused on multipath estimation, including studies of the performance of estimation approaches based on the use of "multicorrelator" delay lock loop (DLL) with an extended Kalman filter as well as an alternative.

Receiver Architecture and Functions

Three main modules comprise the GARDA receiver architecture designed by AASI.

Antenna and RF front-end. This is a single element covering both the lower band (E5, E6) and the higher band (L1). The antenna is designed by Satimo targeting the professional/safety-of-life receiver applications. The active section is based on a Low Noise Amplifier and filters providing required amplification with very good noise characteristics.

RF/IF section. The radio frequency/intermediate frequency section is in charge of RF signals amplification, RF to IF down-conversion and local oscillator synthesis. The down-conversion is based on a single mixing stage, while the final conversion to baseband is accomplished, after the signal digitization, by the digital channel. The IF signal sampling is also performed within this section, using a high speed ADC and coding the samples on three bits.

Digital section. AASI designed and developed a new proprietary digital channel specifically to process Galileo and GPS signals. The channel, named GALVANI, was designed and simulated through a Simulink design process and ported to Very High Speed Integrated Circuit Hardware Description Language (VHDL) for implementation on either of two field programmable gate arrays (FPGAs) — one, an older version with 8 Mgate capacity and the other, an enhanced, higher-capacity version.

The digital section includes a digital signal processor (DSP) that runs all the acquisition signal processing and tracking loops software. Digital channels can be flexibly configured as single-frequency channels (SFCs) including data and pilot signals or as complex multi-frequency channels (MFCs), each handling multiple Galileo carriers. Figure 1 shows a block diagram of the receiver layout.

The receiver model has been tailored to high performance, professional and safety-of-life applications. The specification addresses a receiver capable of processing the Galileo signals on the

GARDAantennapre-industrialprototype covered by its radome

GalileoReceiverPrototypeassembly

L1, E5a, E5b, and E6 bands and the L1 GPS satellite-based augmentation system (SBAS) from the European Geostationary Navigation Overlay Service (EGNOS) and the Wide Area Augmentation System (WAAS).

The new GPS L5 and GPS L2C signals are not currently included in this receiver specification. However, future safety of life (SoL) products may be configured to run three frequencies, including GPS L1-L5 and Galileo L1-E5b. The current receiver implementation allows a SoL application tracking in parallel 10 dual-frequency L1-E5b Galileo SVs, 10 single-frequency L1 GPS SVs and 2 EGNOS/WAAS L1 SVs for a total of 32 single-frequency channels.

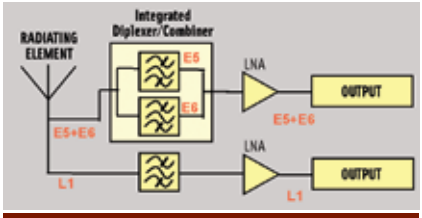


FIGURE 2 AntennaandRFFEBlockDiagram

The receiver main functions include:

- Search visible Galileo/GPS/SBAS SVs, allocate hardware channels according to cold/warm/hot start strategies and predict tracking list using calculated position information
- Acquire and track Galileo/GPS/EGNOS specified signals
- Monitor receiver health status
- Maintain code lock and carrier lock, demodulate and decode data messages, and recover navigation data from each received GNSS satellite
- Implement interference and multipath mitigation techniques (signal processing)
- Perform PVT calculation with GPS, Galileo, and/or a combined GPS+Galileo space vehicles (SVs)
- Perform integrity related calculations (xPL, HMI, critical satellites prediction, and navigation warning) to alert the user in case of integrity risks (only safety-of-life applications)
- Provide raw measurements data for each GNSS satellite in lock
- Allow receiver control by the user through its command & control interface.

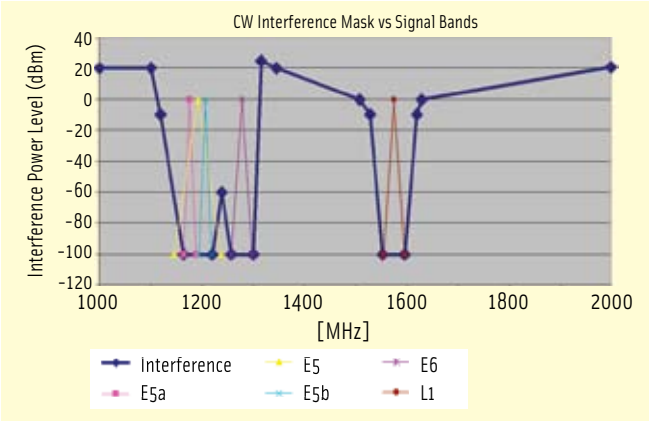


FIGURE 3 Interference rejection mask

Prototype Development

The prototype developed in the GARDA project is a full AASI design. The receiver was initially aimed at verifying the Galileo signal processing capabilities on the four Galileo RF Frequency Channels (L1, E5a, E5b, E6) with the Galileo SIS Interface Control Document (ICD) evolving from issue 7 up to issue 11. The first receiver configuration involved a single SV multi-frequency channel (MFC) with complete acquisition and tracking capabilities. AASI developed and tested new signal processing algorithms, optimized for the Galileo signal modulations.

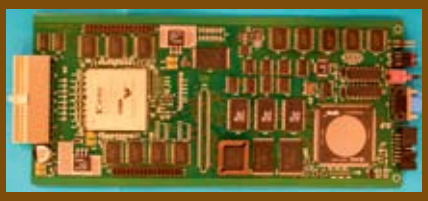
In subsequent configurations, the GALVANI FPGA has been extended to handle signals from eight parallel SVs in dual-frequency configuration to meet the GIRASOLE project needs. With the current design, this is the maximum number of dual-frequency SVs that can fit on the smaller capacity FPGA. The new signal processing board generation instead hosts the new generation FPGA that allows a increase of this number up to 32 channels, configurable into dual-frequency or single-frequency SVs.

The GIRASOLE receiver prototype is now being completed with navigation processing software running GPS-only, GPS+EGNOS/WAAS, and GPS+EGNOS/WAAS+Galileo solutions, in addition to integrity processing SW for the safety-of-life applications.

Antenna and Front End

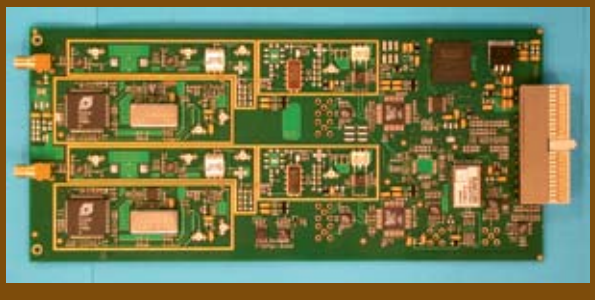
The antenna breadboard design has been driven by the following concepts: phase center stability, minimization

Galileo Receiver Prototype boards



GARDA Receiver DSP Board

GARDA Receiver RF/IF Board (below)



of multi-path and overall phase error, suppression of unwanted out-of-band signals, and minimization of manufacturing costs.

The antenna is a broadband element covering the L1, E5, and E6 bands. Based on a patch element, it includes the input RF filter, for interference mitigation, derived from a custom-made diplexing element. The low noise amplifiers (LNAs) are physically located in the antenna envelope and provide two separate outputs feeding the RF/IF board. (See Figure 2.) Band separation is achieved through the diplexer with reasonable rejection slope and low losses.

The additional separation between the E5 bands is accomplished after the LNA. The interference rejection mask considered in the design is shown in Figure 3.

The GARDA antenna pre-industrial prototype includes also a single-piece metallic cavity. The radome is made out of epoxy resin and glass fibers. The metallic cavity is aluminium coated with alodine.

The back side of the prototype antenna is equipped with two N-output connectors for E5-E6 and L1 bands. The mechanical interface for mounting on a mast is composed of 8xM4 screw holes. Two five-millimeter diameter holes are also present for evacuation of potential condensing humidity inside the antenna.

The performance of this antenna have been verified during the electrical and environmental tests performed on the pre-industrial prototype. The electrical tests cover S-parameters, radiation pattern, calibration of phase center, spectrum, power, and radiated and conducted emissions EMC tests. The environmental tests cover thermal cycling, sine vibration, random vibration, and free fall tests.

The measured gain is presented in Figure 4 and Figure 5 for the center frequencies of E5 and L1 bands. The measured gain throughout the test campaign is shown in Figure 6 for the E6 band, also at the center frequency.

The prototype successfully survived the environmental tests (thermal cycling, vibrations, and shocks). Measured electrical results have also confirmed the high level of performance and stability of the design.

Overall then, the measured performance of the antenna complies with the initial antenna specification.

RF/IF Section

The design of the RF/IF section includes the hardware for two complete signal paths with identical architecture. Each path is in charge of generating the local oscillator (LO) signal, mixing the incoming RF signal to intermediate frequency, according to a properly defined frequency plan, providing the signal amplification, filtering and, finally, digitizing the IF signal.

The down-conversion is based on a single mixing stage, while the final conversion to baseband is accomplished after the signal digitization, by the digital channel. Reconfigurable phase-locked loops (PLLs), image filters, IF filters, and digitally controlled AGCs are located in each signal branch.

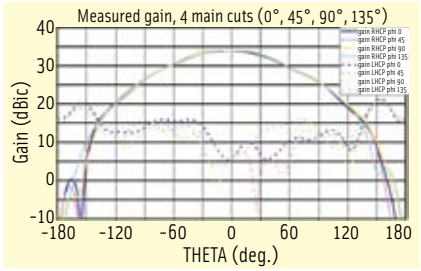


FIGURE 4 Measured gain, f=1191.795 MHz (centerE5),activeantenna,pre-industrial prototype

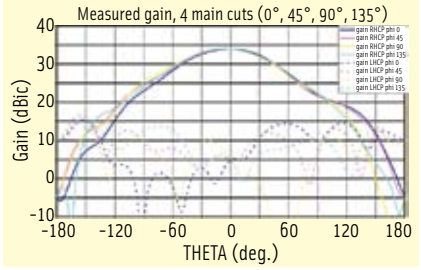


FIGURE5 Measuredgain,f=1575.42MHz(center L1),activeantenna,pre-industrialprototype

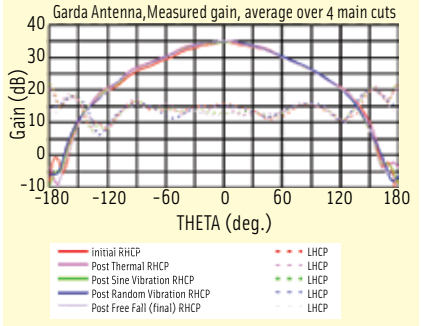


FIGURE6 Measuredgainthroughoutthetest campaign, f=1278.75 MHz (center E6)

The IF signal sampling is also performed within this section, using a high speed ADC. The ADCs have a maximum resolution of 8 bit at 250 Msps, which

also provide low-voltage differential signaling (LVDS) outputs suitable for signals transfer to the signal processing section. The digital samples are coded using three bits and the sampling frequency of the ADC is 95 MHz. This sampling frequency has been selected adopting precautions against aliasing and excess signal loss.

Developing the frequency plan gave consideration to spurious frequency suppression. This means that harmonics or non-harmonics related to the clock generation and mixing process are kept under control and possibly located in non-dangerous frequency regions. The LO and frequency synthesizer have been designed with the goal of achieving optimal phase noise performance. The master oscillator is a standard 10 MHz clock, and the choice of 70 MHz as IF frequency has allowed the use of standard surface acoustic wave (SAW) filters.

Digital Signal Processing

The digital signal processing board is an AASI reprogrammable computing platform for high data-throughput signal processing Galileo/GPS applications. The module can process an entire Galileo/GPS digital channel acquired via LVDS Interface.

In the GARDA configuration, the digital correlation blocks (GALVANI channels) have been developed in VHDL on a version of the earlier-generation FPGA, while signal processing algorithms run on a 32-bit Super Harvard ARChitecture (SHARC) DSP. The board is also equipped with serial peripheral interface (SPI) and RS232 connectors. The former is used to connect an external memory card useful for testing purposes, while the latter is used to download data and code and implements the communication with the user interface program.

Digital channels architecture. The reference block diagram of the GALVANI chip is sketched in Figure 7 it is made up by a matrix of processing elements referenced as a single frequency channel (SFC). Each SFC processing element is dedicated to a particular Galileo carrier and is a flexible processing unit that can be configured and controlled to demodulate and track any channel of the Galileo signal, including both pilot and data sub-channels.

Software running on the DSP core controls and configures the SFC matrix in order to implement acquisition and tracking algorithms and symbols demodulation. In line with this notation, a collection of four SFC elements, one for each carrier, comprise an MFC, which can track all the frequencies from a Galileo satellite.

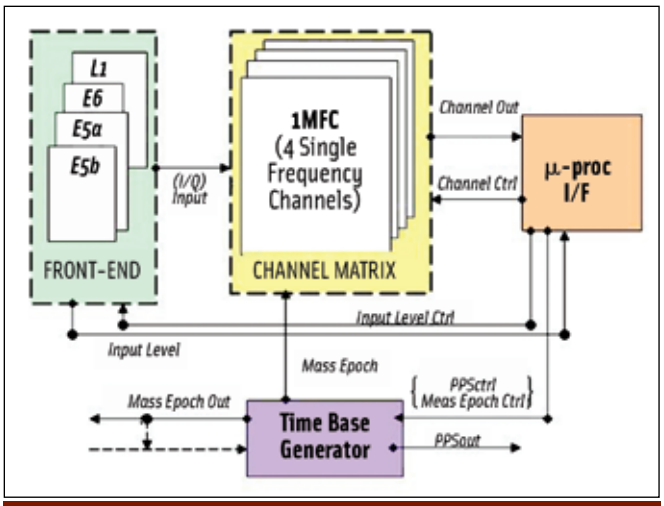


FIGURE 7 GALVANI Digital Channels Block Diagram

For dual-frequency receivers a dual-frequency channel (DFC) is easily built with two SFCs. Channels within an MFC/DFC can be dynamically assigned by software to a common input signal IF in order to increase the number of parallel search correlators during the acquisition phases.

The GALVANI architecture was first designed and simulated on a Simulink bit-true simulation software and then translated into VHDL code. Objects of two hierarchical levels comprise the core, an SFC that implements all the modules necessary for despreading a single signal (code replica generation and correlation), each including in parallel Galileo data and pilot channels; at top level an MFC that implements a coordinative tracking over multiple single-frequency channels.

The SFC main components are:

- a *real to complex converter*, in charge of transforming the IF digitized signal into I/Q components
- the *carrier removal* that performs the final down conversion and removes the residual carrier
- the *code generation unit* in charge of producing the local replica of the spreading codes for both data and pilot sub channels. The CGU is based on memory-stored codes for the primary and secondary codes of data and pilot sub-channels. This allows maximum flexibility versus signal evolutions
- The *code delay line* is composed by the Shift Register block that produces Early and Late versions of the replica code, and by a correlation line with complex correlators for each replica. Five replicas and, therefore, five complex correlators are implemented to allow acquisition, multipath rejection and secondary peaks detection algorithms
- The *time base generator* generates timing signals for common measurement epoch and PPS.

Currently the design of one MFC (with four SFCs) occupies about 5,284 slices, which is approximately 11 percent of the FPGA device.

Signal processing software. The acquisition and tracking of received signals is implemented by DSP software and includes the following functionality: acquisition strategy, tracking Loops (code and carrier), lock detection, data decoding, and raw measurements processing

The current signal acquisition strategy is based on a serial search of the signal power over a bi-dimensional grid on code phase delay domain and frequency domain. The grid bin width in the code domain is one half slot, while the frequency domain is scanned with steps inversely proportional to the integration time.

During acquisition stage all 10 correlators of a single SFC (data+pilot subchannels) can be used simultaneously to scan the code domain of each satellite carrier. In order to avoid false acquisition lock on side peaks of BOC modulation, a "bump and jump" technique is implemented between acquisition and tracking phases. Code tracking is performed by a second order DLL, while a third order PLL is in charge of synchronizing the phase and frequency of the carrier to the incoming signal.

Software Simulator

A software receiver simulator is a key element in the GARDA project. The simulator, developed and subsequently commercialized by one of the GARDA consortium members, has a dual role: test-bench for integration and evaluation of receiver technologies including integration and analysis of user defined algorithms on one side, and SW receiver as asset for GNSS application developers on the other side.

The software simulator is conceived as a modular and configurable tool, in which users can embed and test their own algorithms with a user-friendly interface. It runs on a standard Windows PC, allowing the maximum use from people not involved in the development. The simulator's software suite includes two complementary tools. Each tool allows performance of different analyses or investigation of specific functions and algorithms of the receiver

Bit-true simulator. The bit-true GNSS software receiver simulator recreates the Galileo signal-in-space and the receiver signal processing chain using a sampled-based simulation approach. Developed in Matlab/Simulink to provide high modularity, it targets receiver experts in the development and analysis of the receiver core technologies. The bit-true tool implements a dual-channel receiver (data and pilot) of a specific Galileo carrier.

The simulator enables analyses and simulations of the receiver critical algorithms and architecture design, such as acquisition and tracking, AltBOC modulation performance, and multipath and interference analysis. It includes a user interface that allows the configuration of all system parameters and the visualization of simulation raw outputs and statistics. The user can obtain C-compiled versions of the Simulink models using autocoding techniques, has achieved a 100 percent performance improvement.

The the bit-true tool simulates all the Galileo channels at the selected carrier frequency. It includes ranging codes generation, data and BOC modulation, IF up-conversion, and transmitter filter design. The transmitter module includes the E5 AltBOC modulation scheme.

The propagation channel receiver allows the simulation of different environmental effects, including additive white Gaussian noise (AWGN), multipath delay, external interference, and system dynamics. The multipath model consists of the sum of a direct ray and several indirect paths affected by a random fading component.

Interference modelling includes band-limited Gaussian noise and GPS interference. The relative dynamics between the receiver and the satellite is considered including both code and carrier Doppler shifts in the transmitted signal.

The receiver is modelled both in floating and fixed-point designs. It includes RF modelling, IF down-conversion, ADC, code acquisition, code and carrier tracking, data detection, and C/N0 estimation.

The receiver architecture is able to simulate any possible sampling frequency or chip spacing. The simulator modular design allows the modification of the default Simulink model and the insertion of user-defined algorithms, receiver architectures, and environment perturbations.

Environment and navigation simulator. The environment and navigation simulator is a Galileo/GPS raw data generator and navigation tool oriented to application developers who need external access to raw measurements or PVT solution. The environment and navigator simulator includes realistic characterization of the effect of the different error components, depending on the type of terminal and GNSS receiver configuration. Users can configure Galileo and GPS constellations, environmental conditions, satellites and receiver parameters, and navigation algorithms.

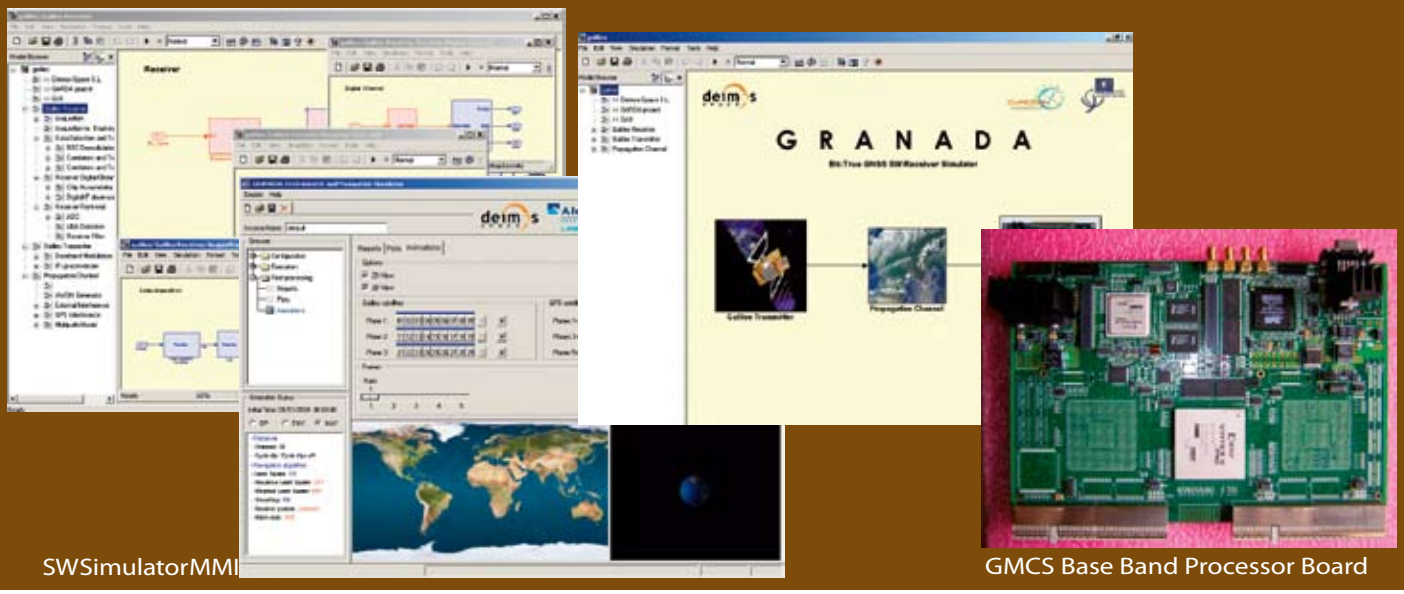
The receiver architecture is able to simulate any possible sampling frequency or chip spacing.

The tool, implemented in C-code, includes a user interface that allows the configuration of all system parameters, execution of the selected case, and the visualization of simulation outputs results.

The software enables the user to simulate the navigation process and analyze the performance of different types of receivers. Pseudorange, carrier phase, and Doppler measurements are generated, taking into account satellites and user receiver dynamics, environmental perturbations, receiver configuration, and selected GPS/Galileo carriers and channels.

Configurable user equivalent range errors are introduced in the generated measurements. Range errors include satellite and receiver clock modelling, user dynamics, ionospheric and tropospheric delays, receiver tracking errors, multipath, relativistic effects, ephemeris errors, and cycle slips. The receiver implements configurable algorithms to correct these perturbations.

The resulting measurements are used to obtain the PVT solution with different navigation algorithms that can be selected in the user interface, including least squares, recursive least squares, and weighed least squares. A carrier-phase smoothing algorithm is also included in the simulator. Both single and dual frequency receivers can be selected. Users can also compute a combined Galileo-GPS navigation solution (selecting satellites from either constellation and applying a criterion for optimization of dilution of precision or DOP).



SWSimulatorMMI

GMCS Base Band Processor Board

Galileo Mono Channel RF Simulator

Laboratory equipment design to faithfully reproduce representative GNSS signals in space provides an indispensable aid to the rapid development and effective performance verification of GNSS receivers. This is particularly true in the case of Galileo, for which space and ground segments are being concurrently developed under a tight schedule. As a matter of fact, despite certain commonalties with GPS, Galileo has specific features that imply the need for an ad hoc development of user receivers.

This was the main rationale behind the GJU decision to require the design and development of a Galileo Mono Channel Simulator (GMCS) within the frame of the GARDA project. The GMCS, designed and manufactured by Space Engineering (Italy), provides a tool, compliant with the Galileo SIS ICD, to support the development and performance assessment of Galileo receivers.

The GMCS is able to generate the three carriers defined in the Galileo SIS ICD that are produced by a single satellite of the constellation — hence, the term "Mono-Channel" simulator. In particular, the GMCS can be configured to simultaneously generate either the L1/E5 or the L1/E6 carrier pairs, taking also into account the various options for message structures. The GMCS also permits the dynamic emulation, according to the satellite and user motion, the main parameters of the transmission channel. These include on-board transmitter non-linearity (amplitude and phase), on-board antenna gain, ionosphere and troposphere behavior, frequency-selective multipath, Doppler, free space loss, in-band interference, and thermal noise.

The GMCS also allows users to fill the message in various modes (user-defined, dummy, autonomous). Furthermore, the simulator is able to work with an internal reference (10.23 MHz) or an external one (10 MHz or 10.23 MHz). The simulator displays the following main performances in terms of errors/uncertainty:

- pseudorange errors (code phase offset) within 5 mm
- pseudorange rate sub-millimeter errors
- pseudorange acceleration errors within 5 mm/s^2
- delta range error (carrier phase change) within millimeters
- modulation uncertainty within 53 mrad.

These features made the GMCS a complete and self-standing test set for validating the GARDA receiver prototype.

GMCS architecture. The GMCS top-level functional architecture is shown in Figure 8. Six different blocks can be identified A *message generator* supports the F/NAV, I/NAV and C/NAV message types and performs the convolutional channel encoding and interleaving. The *transmitter section* performs the modulation, interpolation, and on-board high-power amplifier(HPA) emulation functions. The *channel section* block emulates Doppler, on-board antenna gain variation, multipath, and white Gaussian noise, as well as the other effects caused by propagation over the free space, the troposphere, and the ionosphere.

A *satellite/receiver motion and geometry* block performs the main functions relevant to the relative satellite/receiver configurations: satellite dynamics, user kinematics, distance, relative velocity, relative acceleration, and relative jerk between the satellite and the receiver, satellite elevation angle with respect to the receiver, angular position of the receiver with respect to the satellite. An *analog front-end* performs the digital to analog conversion and the RF up-conversion.

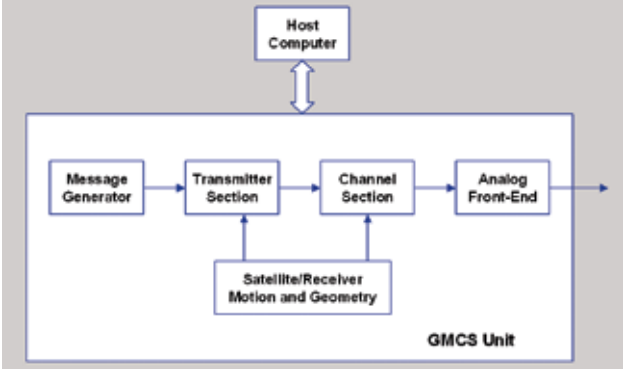


FIGURE 8 GMCS Functional Architecture

GMCS RF Modulator

GMCS Rack Front Panel

The *host computer* implements the graphical user interface, the main panel of which is shown in Figure 9.

GMCS implementation approach. The GMCS pursues an almost fully digital implementation, which yields very high flexibility and accuracy. It comprises the following main items pictured in the accompany photos:

- the digital hardware platform, consisting of a custom baseband processor board, two DAC board assemblies, and a custom backplane
- the custom up-conversion board, performing modulation, filtering and conversion onto L-band, specifically designed and manufactured for Galileo signal emulation
- other COTS items: mainly clock generators, processors, communications interface, an external PC, a 19-inch rack with a power supply system.

GMCS Tests Results. The GMCS requirements have been verified using the inspection, design, analysis, and test methods in two main set-ups: connecting the GMCS RF output to a spectrum analyzer digital fast-fourier transform based on a 20 Gsps true sampling scope with six GHz of analog bandwidth; connecting the GMCS DAC board output to a logic state analyzer.

Forty different tests have been performed. Figures 10-12 show the results of the first one, demonstrating the simultaneous generation of L1, E5, and E6 signals with the expected power spectra.

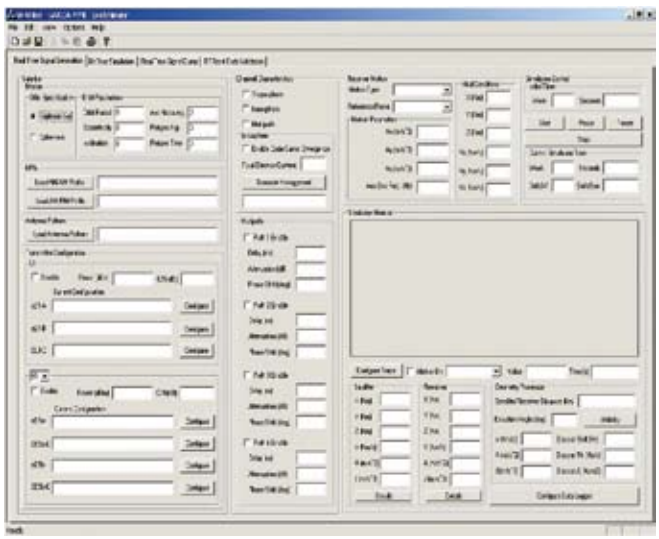


FIGURE 9 GMCS GUI

GARDA Receiver Test Results

In addition to verification of the acquisition and tracking functionality performed in May 2006 with the GIOVE-A Galileo Satellite Testbed–V2 satellite, the GARDA receiver prototype has been tested using several types of laboratory test equipment.

FIGURE 10 L1 Power Spectrum

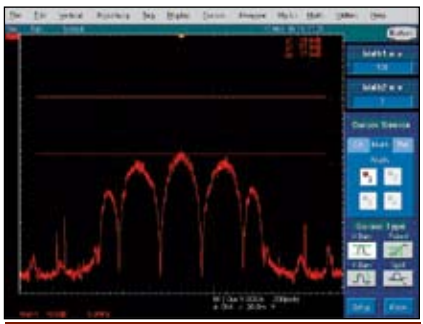
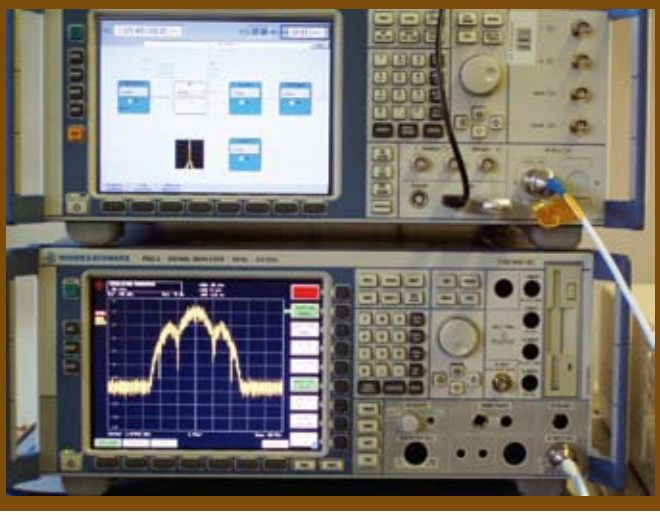


FIGURE 11 E6 Power Spectrum

FIGURE 12 E5 Power Spectrum



(above) Prototype Galileo Simulator used for Rx functional & performance tests
(left) Vector Signal Generator used for Rx boards tests

Initial testing of the DSP and GALVANI has been conducted using a test memory board that can be directly connected to the DSP/FPGA. This setup has allowed us to test the basic functionality of the digital channels. The memory is loaded with I/Q samples generated by the bit-true SW simulator at IF.

In a second step, a vector signal generator was used in order to create an RF signal with all Galileo modulations connected to the antenna front-end, stimulating the RF chains.

Receiver functional and performance testing was conducted using the GMCS and several commercial Galileo single- and multi-channel RF signal simulators.

The available Galileo multi-channel simulator is able to transmit signals for a constellation of Galileo SVs on the L1 and E5 bands. The GMCS is able to transmit a single SV signal on all the Galileo carriers. The following receiver performance have been characterized in particular: signal and noise measurements, acquisition performance, tracking thresholds characterization, code and carrier phase noise, and signal and tracking dynamic limits

Signal and noise measurements. Calibrating the output signal power of the simulators and comparing with the measured C/No at the output of the receiver correlators, it is possible to compute an estimate of the implementation loss of the complete receiver chain (from antenna front-end to correlators). On the L1C signal this value is shown to be in the order of less than 2 dB. The same measurement performed on E5a and E5b shows implementation losses that are higher by about 1-2 dB.

The receiver chain implementation loss is explained by the fact that the implemented tracking algorithm is single-side band. The input signal is demodulated to the respective side-band centers of E5a and E5b, using sub-carrier free reference signals and after a band-limitation to 40 MHz. Calculating the cross-correlation function with the unfiltered input signal and the band-limited reference signal, the correlation losses are expected to be about 1.2 dB. (See Figure 13.)

Code and carrier phase noise. Code phase noise was measured by subtracting the carrier phase measurements, removing the constant part and taking the standard deviation. For L1 a perfect match with John Betz and James Spilker theoretical formulas has been obtained, while for E5A a degradation of approximately 1.5 dB is seen. (See the Additional Resources section at the end of this article for full reference details of the Betz and Spilker articles.)

Carrier phase noise is computed by subtracting two carrier phase measurements on two different satellites in order to eliminate the phase noise of receiver and simulator clocks. After this operation, differenced data has been processed through a second-order polynomial fit to remove signal dynamics. Finally, the standard deviation is divided by the square root of two because of the contribution from two satellites transmitting exactly the same power. As for the code phase measurements, L1 and E5 results also match the theoretical expectations quite well. (See Figures 14 and 15.)

Acquisition performance. The main objective of acquisition performance tests was to verify the signal acquisition probability within the time of one code

C/No [dBHz]	Signal	Pd [%]
31	L1c	85.7
34		94.3
37.5	E5a-Q	100
37.1	E5b-Q	100
37	E6c	69

TABLE 3. Measured Acquisition Probabilities

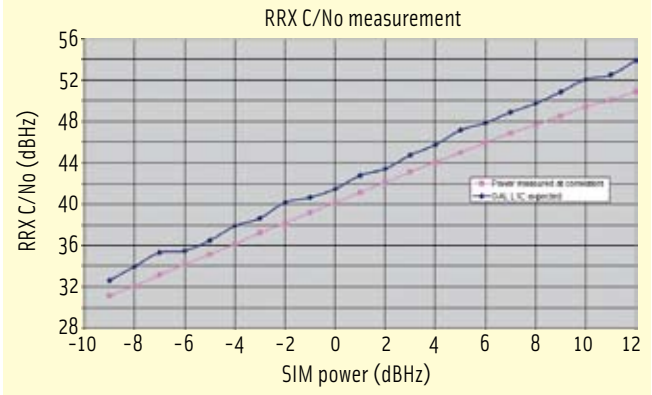


FIGURE 13 Rx C/No Measurements on L1C

scan over a Doppler frequency bin. Table 3 shows the acquisition probabilities (Pd) obtained and the related C/No.

Tests on acquisition performance also allowed us to verify side-peak false acquisition behavior. The technique used in the stage between acquisition and tracking removes the majority of false acquisitions: the proportion of false acquisitions is about 2.5 percent at 33 dBHz (Figure 16).

Tracking thresholds characterization. Tracking threshold tests were carried out to obtain the receiver tracking C/No lower limit. This test consists of quickly dropping signal power down to 30 dBHz and then, from that point, further in reducing power slowly (1dB/30sec). The threshold is measured as the minimum C/No at receiver correlators for which the receiver channel is able to maintain a continuous tracking 95 percent of the time. Results in Table 4 show that the receiver loss of lock is on the order of 20 dBHz.

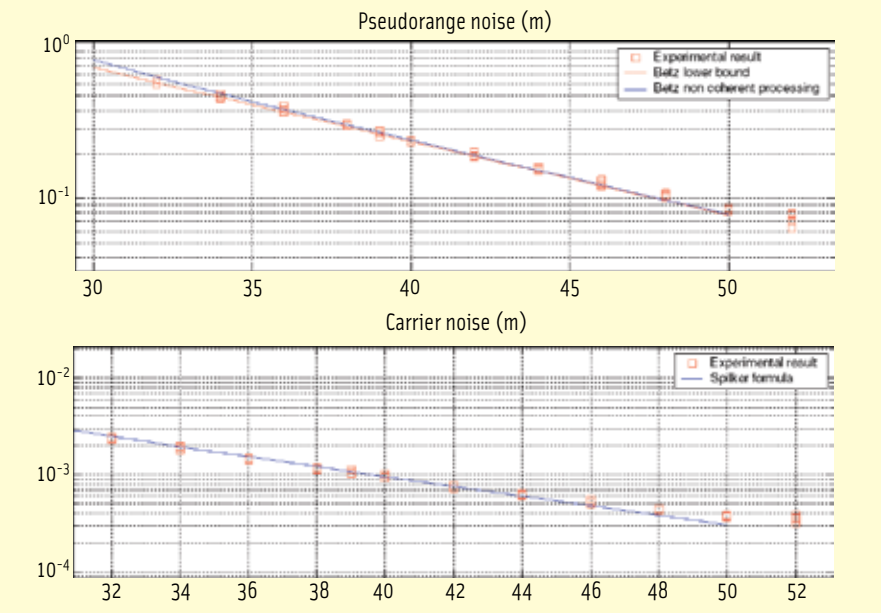


FIGURE 14 Pseudorange and carrier thermal noise measurements on L1C

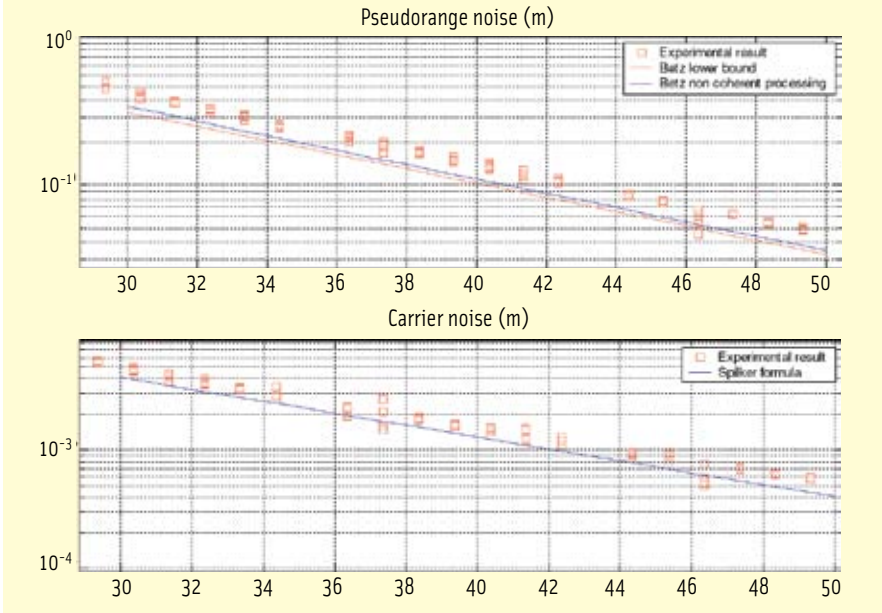


FIGURE 15 Pseudorange and carrier thermal noise measurements on E5A-Q

Loss of lock at signal to noise ratio [dBHz]				
	L1c	E6c	E5a-Q	E5b-Q
Average	20.2	19.7	19.5	19.8

TABLE 4. Loss of lock thresholds

Conclusions

The GARDA project has presented the opportunity to develop some basic Galileo technology components. The GARDA receiver is one of the first Galileo receivers, and this experience is at the basis of several on-going projects and future AASI receiver product lines:

- the GIRASOLE Safety of Life receiver will be the pre-cursor of a combined GPS/Galileo receiver product to be used in rail, aviation, and maritime applications. First demonstrations are expected to be carried-out in the frame of the GJU second call for the GRAIL project for rail applications
- building blocks from the GARDA design are being re-engineered for use within the Galileo reception chain receiver (GRC), which is a key element of the Galileo Mission Segment ground infrastructure
- building blocks from the GARDA design are also being re-engineered for the test user receiver that will be employed to assess the performance of Galileo during the in-orbit validation phase

Furthermore, the software simulator toolkit as well as the Galileo RF signal simulator are available to Galileo receiver and user applications and will be further improved to incorporate additional features.

Manufacturers

The Galileo Receiver Analysis and Design Application (GRANADA) simulation toolkit from **Deimos Space**, Madrid, Spain, with its Bit-True GNSS Receiver Simulator and Environment and Navigation Simulator has provided design and testing support throughout the GARDA project.

The Galvani IC was implement on Virtex2 and/or Virtex4 FPGAs from

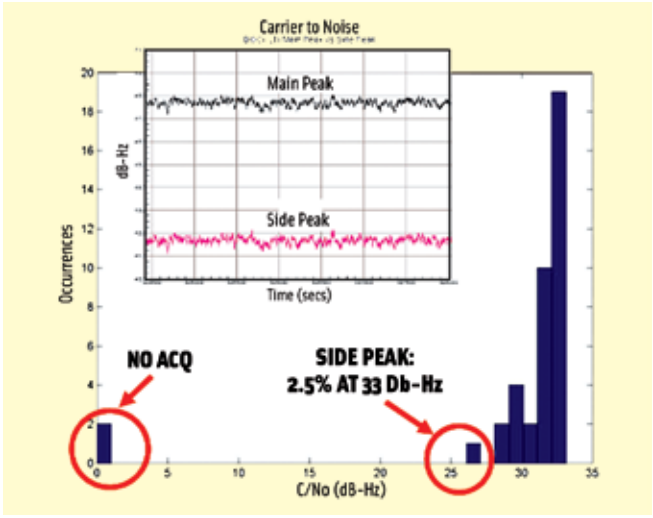


FIGURE 16 Side Peak False Acquisition at 33dBHz

Xilinx, Inc., San Jose, California, USA. In the GARDA configuration, the digital correlation blocks (GALVANI channels) have been developed in VHDL on a Virtex-II XC2V8000 FPGA from Xilinx, while signal processing algorithms run on Analog Device ADSP-21060 SHARC from **Analog Devices, Inc.**, Norwood, Massachusetts, USA. The digital section includes an Analog Devices ADSP21x60 digital signal processor that runs all the acquisition signal processing and tracking loops software. The ADCs used are AD9480, also from Analog Devices.

The GMCS DAC board assemblies are based upon the DSP Builder development tool from **Altera Corporation**, San Jose, California, USA. The GMCS test configurations used a 20 Gsps true sampling scope from Tektronix Inc., Beaverton, Oregon, USA, and an HP 16500C Logic Analysis System from **Agilent Technologies**, Santa Clara, California USA.

The GARDA receiver was tested using Spirent 4500 and 7700 GPS simulators and the Spirent Prototype 7800 Galileo simulator, **Spirent Communications**, Paignton, Devon, England, as well as the Galileo Mono Channel Simulator developed in the frame of the GARDA program by **Space Engineering**, of Rome, Italy.

Additional Resources

[1] www.garda-project.it

[2] www.girasole-project.it

[3] http://www.deimos-space.com/granada/

[4] Betz, J.W. (2002), Binary Offset Carrier s for Radionavigation, Navigation: Journal of the Institute of Navigation, Vol. 48, Number 4, pp. 227-246

[5] Spilker, J.J., Global Positioning System: Theory and Applications. Vol. 1

Authors

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Gianluca Franzoni received an electronic engineering degree from the University of Pavia, Italy. From 1988–90 he was with Marconi Italiana S.p.A. and then joined Laben S.p.A (now Alcatel Alenia Space). Franzoni worked as a system engineer for many space application programs before starting his activity in the GPS applications–related field. In particular he has been working as project leader for the design and development of GPS receivers for space applications, both single- and dual-frequency, including the GPS Tensor receiver for Globalstar, Proteus GPS receiver for ATV, and the LAGRANGE and GOCE SSTI receivers. He is currently the project leader for the GARDA and GIRASOLE Galileo receivers.

Dario Fossati received his master's degree in mathematics from the University of Milan. He leads the Power and Processing Department of the Alcatel Alenia Space Italia, Industrial Unit in Milan. He has been involved in GNSS products and technologies since 1995, leading teams for the development of both GPS and dual standard GPS/GLONASS receivers for ground and space application. He was responsible of the GARDA Project.

Lucio Foglia received a master's degree in nuclear engineering from Politecnico of Milano, Italy. He led the VLSI design group at Laben S.p.A. Since 2002 he has been involved in navigation programs. Currently Foglia is in charge of navigation ground equipment development within the Navigation and Integrated Communications Business Unit of Alcatel Alenia Space Italia and program manager of the GIRASOLE project.

Vincent Gabaglio holds a Ph.D. in technical sciences and M.Sc. in surveying engineering from the Ecole Polytechnique Federale of Lausanne (EPFL). He has research experience at the EPFL Geodetic Engineering Laboratory and the Satellite Navigation & Positioning (SNAP) group at the University of New South Wales, Sydney, Australia. Involved in the Galileo project since 2001, Gabaglio now works in the Galileo Joint Undertaking as R&D officer, in charge of the 6th Framework Programme Research & Development activities related to Galileo. He previously held responsibilities for the GNSS application and receiver development.

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Luc Duchesne obtained a diploma of Engineering in general electronics in 1992 from ENSI, Angers-F, and then a master's degree in aerospace electronics in 1994 from Supaéro, Toulouse-F. He worked six years at DASA (now Astrium-EADS) in Munich where he developed several space antenna systems and subsystems from L-band to Ka-band. Since 2000 he as served at SATIMO as the director of the research and development department. Besides studies for CNES, ESA and GJU, he has supervised the development of several products such as the portable antenna measurement system called StarLab functioning over the 800 MHz–18 GHz band or the non destructive testing system at X-band for quality control of scrolling materials on production lines.

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Antonio Fernández received his M.S. degree in aeronautical engineering from the Polytechnic University of Madrid in 1994. He has been working in the field of GNSS since 1996. Fernández co-founded DEIMOS Space in 2001, where he is currently in charge of the GNSS Technologies Sec-

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tion in the Advanced Projects Division. In 2003, he obtained an M.S. in physics from the UNED University of Spain.

Augusto Caramagno obtained his M.S. degree in electronic engineering from the University of Catania, Italy, in 1994. He co-founded DEIMOS Space in 2001 and is today the head of the Advanced Projects Division and senior project manager coordinating the Engineering activities in DEIMOS Space and DEIMOS Engenharia.

Robert Schweikert received his Diploma and his Ph.D. degree in physics from the University of Frankfurt/Germany. He joined the Institute for Communications Technology at the German Aerospace Centre (DLR) in 1978 and became head of the communication systems and of the communication theory department as well, in 1983 and 1992, respectively. Spent one year at INTELSAT in Washington D.C./USA in 1991/1992. In 1998, he founded the AUDENSACT Consulting GmbH with his partner Thomas Wörz, where he acts as managing director. His expertise comprises various areas of communications and satellite navigation including system analysis & design, (wireless) propagation channel analysis and modelling as well as applications of spread spectrum techniques.

Thomas Wörz received a Diploma from the Technical University of Stuttgart/Germany, a Ph.D. degree in electrical engineering from the University of Munich/Germany. He joined the Institute for Communications Technology at the German Aerospace Centre (DLR) as research staff member in 1988. In 1998, he founded the AUDENSACT Consulting GmbH with his partner Robert Schweikert, where he acts as managing director. His expertise comprises analysis and modelling of mobile satellite and terrestrial wireless channels, signal structures and corresponding receiver design. IG

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